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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/762,975	01/22/2004	Alexander G. MacInnis	17403US04	6110

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EXAMINER	
MYERS, PAUL R	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 05/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/762,975	MACINNIS ET AL.	
	Examiner	Art Unit	
	Paul R. Myers	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/18/06-1/13/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-3, 6-7, 9-12, 14-15, 25-27, 29-31, 33-34 are rejected under 35 U.S.C. 102(e) as being anticipated by Meinerth et al PN 6,199,149.

In regards to claims 1, 27, 31: Meinerth teaches a scheduling apparatus capable of providing an interface between a memory (either system memory or local memory) and at least a first (122) and second device ("other system devices" The processor is included as an other device), the scheduling apparatus comprising: a memory request arbiter (inherent the requests for the memory have priorities) capable of controlling access to the memory by different devices having different priorities (Abstract); and at least one counter (408) coupled to the memory request arbiter, wherein the at least one counter is associated with at least the first device (The overlay engine) of the at least two devices, and wherein the at least one counter enforces a time-period that precludes access by the first device to the memory (Abstract).

In regards to claims 2, 12, 29, 33: Meinerth teaches neither the overlay engine nor the processor have per-determined periodic behavior.

In regards to claims 3, 25, 26, 30, 34: Meinerth teaches the overlay engine has expedited processing priority and is sensitive to latency.

In regards to claim 6: Meinerth teaches the first device is a graphics device.

In regards to claim 7: Meinerth teaches the devices include a CPU and a graphics device.

In regards to claims 9, 10: Meinerth teaches the graphics device including accelerated graphics and a display engine.

In regards to claim 11: Meinerth teaches the graphics device is high priority.

In regards to claim 14: Meinerth teaches the counter is programmable (Column 1 lines 53-57).

In regards to claim 15: Meinerth teaches the time period is set in response to a memory access request.

3. Claims 27-28 and 31-32 are rejected under 35 U.S.C. 102(e) as being anticipated by Ajanovic PN 6,199,127.

In regards to claims 27, 31: Ajanovic teaches a scheduling apparatus capable of providing an interface between a memory (160) and at least two devices (140, 150, 170), the scheduling apparatus comprising: a memory request arbiter (112) capable of controlling access to the memory for different devices having different priorities; and at least one counter (210) associated with the memory request arbiter, the counter using time-periods during which at least one of the devices will not have high priority access to the memory.

In regards to claims 28, 32: Ajanovic teaches reducing the priority of the high priority request for a time period (Abstract).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 4-5, 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jinzaki PN 4,975,833 in view of Temple 5,937,199.

In regards to claim 1: In regards to claim Jinzaki teaches a scheduling apparatus capable of providing an interface between a memory (either of the local memories 21 or 22) and at least a first (11) and second device (12), the scheduling apparatus comprising: a memory request arbiter (31,32,41 and 42) capable of controlling access to the memory by different devices. Jinzaki teaches alternately allowing/prohibiting access to the memories by the processors and prohibits a first processor from accessing a memory again until after the other processor has accessed the processor (Column 4 lines –33). Jinzaki does not teach the processors having priorities or a counter coupled to the memory request arbiter, wherein the counter is associated with at least the first device of the at least two devices, and wherein the at least one counter enforces a time-period that precludes access by the first device to the memory. Temple teaches requests associated with multiple requesters each having its own counter for masking the request from being again servicing the request until the counter has timed out and each request having its own priority. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include a counter for time out because this would have allowed for the memory to again be freed for accessing by a first processor in the case that the second processors fails to

again access the memory because this would have prevented lockup due to a single processor error. Jinzaki also teaches more than just 2 processors but does not indicate how to handle multiple requests from more than one "second" processors at the same time. The purpose of priorities is to handle this situation. It would have been obvious to include priorities with the requests because this would have allowed for servicing simultaneous requests from multiple alternate processors.

In regards to claim 4: Jinzaki teaches the device being a CPU.

In regards to claim 5: Temple does not teach what priorities are assigned to what devices. Official notice is taken that processors routinely are high priority. It would have been obvious to a person of ordinary skill in the art to have a processor have a higher priority.

In regards to claims 16-19: Jinzaki teaches the requests timing being controlled by memory accessing by the other processor.

6. Claims 8, 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Meinerth PN 6,199,149.

In regards to claim 8: Meinerth does not teach the graphics device being incorporated in the same IC chip as the scheduler. Official notice is taken that integrated circuits chips are well known. It would have been obvious to a person of ordinary skill in the art at the time of the invention to integrate the scheduler and graphics device in the same IC chip because this would have decreased the physical size of the system. See also MPEP 2144.04 V B.

In regards to claim 13: Meinerth teaches the device being "other device", however Meinerth is silent upon whether the other device has a determinable periodic behavior. Official

notice is taken that many other devices are known that have determinable periodic behavior are known such as a memory refresher (Used to refresh memories that require periodic refreshing). It would have been obvious to include a device that has a determinable periodic behavior because this would have prevented limiting the system of Meinerth.

7. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Meinerth PN 6,199,149 in view of Kaplinsky et al PN 4,782,462.

In regards to claim 20: Meinerth teaches the device including a graphics device or "other devices". Meinerth does not expressly teach the graphics device including a window controller. Kaplinsky et al teaches that a graphics device normally includes a window controller that has memory access requests. It would have been obvious to a person of ordinary skill in the art at the time of the invention to have the graphics device include a window controller or alternatively have one of the "other devices" be a window controller because this would have allowed for rasterizing the images.

8. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Meinerth PN 6,199,149 in view of Kaplinsky et al PN 4,782,462.

In regards to claim 21: Meinerth teaches the requests being sent with priorities, however Meinerth is silent upon the exact handling of the requests. Bass et al teaches a server coupled between device including scheduling tasks with requests. It would have been obvious to have the arbiter also accept other requests such as tasks from a server because this would have allowed for a more robust system including multiple jobs.

In regards to claim 22: Bass teaches the tasks can be scheruled in a round robin method.

In regards to claims 23, 24: Meinerth teaches the graphics overlay having expedited priority (aka highest priority), thus the tasks must comparatively have low priority.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul R. Myers whose telephone number is 571 272 3639. The examiner can normally be reached on Mon-Thur 6:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul R. Myers

PRM
May 4, 2006

PAUL R. MYERS
PRIMARY EXAMINER